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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,629	12/30/2003	Akira Kakizawa	42P17985	9841
8791 75	590 06/14/2005		EXAM	INER
	OKOLOFF TAYLOR RE BOULEVARD	TANG, MINH NHUT		
SEVENTH FLOOR			ART UNIT	PAPER NUMBER
LOS ANGELE	S, CA 90025-1030		2829	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		180
	Application No.	Applicant(s)
Office Antique Comments	10/749,629	KAKIZAWA ET AL.
Office Action Summary	Examiner	Art Unit
	Minh N. Tang	2829
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the o	correspondence address
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a repl If NO period for reply is specified above, the maximum statutory period - Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailin earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be tirely within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).
Status	•	
1)⊠ Responsive to communication(s) filed on <u>01 A</u>	pril 2005.	
· · · · · · · · · · · · · · · · · · ·	s action is non-final.	·
3) Since this application is in condition for allowa		osecution as to the ments is
closed in accordance with the practice under	and the second s	
Disposition of Claims		
4)	are withdrawn from consideration . rejected.	
Application Papers		
9) ☐ The specification is objected to by the Examine 10) ☑ The drawing(s) filed on 30 December 2003 is/a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the Example 2003.	are: a)⊠ accepted or b)⊡ objec drawing(s) be held in abeyance. Se tion is required if the drawing(s) is ob	e 37 CFR 1.85(a). ejected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119	•	
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Burea * See the attached detailed Office action for a list	ts have been received. ts have been received in Applicat ority documents have been receiv u (PCT Rule 17.2(a)).	ion No ed in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/02/04.	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal f 6) Other:	

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DETAILED ACTION

Election/Restrictions

- 1. Applicant's election of the species of Figs. 1 and 4 (claims 1-6, 9-14, 18-24) in the reply filed on April 01, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
- 2. Claims 7-8 and 15-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on April 01, 2005.
- 3. Claims 5-6, 13-14 and 21 are further withdrawn from further consideration by the Examiner because those claims are not readable on the elected species.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on July 02, 2004 is considered by the examiner. It is noted that the U.S. reference 6,725,406 are listed twice, therefore one of those identical U.S. reference is crossed out.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 1, 9, 11, 18 and 19 are objected to because of the following informalities: a/ in claim 1, since there is insufficient antecedent basis for the limitation "the

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selected pin" (lines 4 and 5), therefore, for examination purpose, a limitation — as a selected transmitter pin — is inserted after "transmitter pin" (line 3).

b/ in claim 9, likewise claim 1, a limitation -- as a selected transmitter pin -- is inserted after "transmitter pin" (line 3).

c/ in claim 11, since there is insufficient antecedent basis for the limitation "the selected termination resistors" (line 3), therefore, for examination purpose, a limitation -- as selected termination resistors -- is inserted after "termination resistors" (line 2).

d/ in claim 18, likewise claim 1, a limitation -- as a selected transmitter pin -- is inserted after "transmitter pin" (line 6).

e/ in claim 19, a limitation followed by linking terms (e.g., can be) is considered indefinite since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. For examination purposes, "can be" (line 5) is interpreted as -- are --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-2, 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bu et al. (U.S.P. 6,809,541).

As to claims 1 and 9, Bu et al. discloses, in Fig. 3, a semiconductor device comprising: a plurality of multiplexers (304) to select one of a positive transmitter pin (i.e., pin with upper-limit voltage V+) and a negative transmitter pin (i.e., pin with lower-limit voltage V-) as a selected transmitter pin; and a first comparator (302) to compare a voltage (Vm) of the selected pin with a first reference voltage (Vr) to determine whether leakage exists at the selected pin.

As to claim 2, Bu et al. discloses in column 4, line 30-33, core logic circuitry (digital testing machine) to receive an output (C(i)) of the first comparator (302).

As to claim 10, Bu et al. discloses in Fig. 3, selecting the first reference voltage (Vr) out of a plurality of voltage supplies (Vr, Vp).

Claim Rejections - 35 USC § 103

- 9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 4, 12, 18, 20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bu et al. (U.S.P. 6,809,541) in view of Rearick et al. (U.S.P. 6,762,614).

As to claims 4, 12 and 20, Bu et al. discloses all the limitations recited in the claims except for a positive receiver pin and a negative receiver pin coupled to the positive and negative transmitter pins, respectively, to provide an analog loop back path. Rearick et al. discloses in Fig. 6D, a positive receiver pin (i.e., pin connected to receiver 614A) and a negative receiver pin (i.e., pin connected to receiver 614B) coupled to the positive and negative transmitter pins (602A, 602B), respectively, to provide an analog loop back path. It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Bu et al. by providing the positive and negative receiver pins as taught by Rearick et al. in order to provide a corresponding outputs to the IC core of the integrated circuit.

As to claim 18, Bu et al. discloses, in Fig. 3, a semiconductor device comprising: a plurality of multiplexers (304) to select one of a positive transmitter pin (i.e., pin with upper-limit voltage V+) and a negative transmitter pin (i.e., pin with lower-limit voltage V-) as a selected transmitter pin; and a first comparator (302) to compare a voltage (Vm) of the selected pin with a first reference voltage (Vr) to determine whether leakage exists at the selected pin. Bu et al. does not disclose a computer system comprising a

plurality of dynamic random access memory devices (DRAM); and a chipset coupled to the plurality of DRAMs. Rearick et al. discloses in Figs. 7 and 8, a computer system (i.e., computer-readable medium) comprising a plurality of dynamic random access memory devices (RAM, ROM, etc.); and a chipset (710) coupled to the plurality of DRAMs (RAM, ROM, etc.). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Bu et al. by providing the computer-readable medium having a plurality of dynamic random access memory devices and a chipset coupled to the plurality of DRAMs as taught by Rearick et al. in order to facilitate automated test equipment functionality for testing integrated circuits.

As to claim 22, Rearick et al. discloses in Figs. 7 and 8, the semiconductor device is a memory controller.

As to claim 23, Rearick et al. discloses in Figs. 7 and 8, the semiconductor device is an input/output controller.

As to claim 24, Rearick et al. discloses in Figs. 7 and 8, a processor coupled to the chipset.

Allowable Subject Matter

12. Claims 3, 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3 and 19 recite, inter alia, a first plurality of termination resistors coupled to the positive transmitter pin; and a second plurality of termination resistors coupled to

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the negative transmitter pin such that each of the first and second pluralities of termination resistors are tested with the first reference voltage and the first comparator.

Claim 11 recites, inter alia, selecting one or more of a plurality of termination resistors as selected termination resistors; and testing the selected termination resistors with the first reference voltage and the first comparator.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Asai et al. 6,150,831 Test Method And Device For Semiconductor Circuit.

Simmons et al. 6,876,218 Method For Accurate Output Voltage Testing.

Communication

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MINH NHUT TANG
PRIMARY EXAMINER

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